WHAT IS CLAIMED IS:

1. A processing method of JPEG 2000 bit modeling with a significance propagation decoding pass, wherein a processing circuit of bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said processing circuit simultaneously generating a context and a decision of data changing according to a state of significance flags of a bit to be processed and ambient bit group and a context and a decision of sign bits changing according to a state of the sign bits of the bit to be processed and the ambient bit group; adopting the context and decision of the sign bits only when a value of the bit to be processed is 1 and updating the significance flag; disposing of the context and the decision when the value of the bit to be processed is 0; and updating a processed flag whether the value of the bit to be processed is 1 or 0.

2. The processing method according to claim 1, said processing circuit comprising:

a register which stores a value of data of a bit to be processed;

a register which stores significance flags and sign bits of the bit to be processed and ambient bit group; and

a register which stores an unprocessed flag of the

bit to be processed.

3. A processing method of JPEG 2000 bit modeling with a magnitude refinement pass, wherein a processing circuit of the bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said processing circuit referring to significance second bit which is information about as to whether or not a bit to be processed is processed with the magnitude refinement pass at first time, a processed flag and an significance flag so as to make a judgment as to whether or not the bit to be processed is processed; and in the case where the bit to be processed is processed with the magnitude refinement pass, generating a context and a decision of the bit so as to update the processed flag.

4. The processing method according to claim 3, said processing circuit comprising:

a register which stores a value of data of a bit to be processed;

a register which stores significance flags of the bit to be processed and ambient bit group; and

a register which stores a significance second bit which is information about as to whether or not the bit to be processed is processed with the magnitude refinement pass

at the first time.

5. A processing method of JPEG 2000 bit modeling with a cleanup pass, wherein a first processing circuit of the bit modeling for, when all bits in Annie group to be processed are unprocessed, makes a judgment as to whether or not the bits can be processed collectively and when all the bits in the group are insignificant, generating a special context and a decision; and a second circuit of the bit modeling for not processing processed bits and processing insignificant bits are provided, and said first processing circuit is applied to one bit and said second processing circuit is applied to four bits in the group simultaneously so as to process the bits in parallel.

6. A processing method of JPEG 2000 bit modeling comprising:

a step of processing a significance propagation decoding pass, wherein a first processing circuit of bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said first processing circuit simultaneously generating a context and a decision of data changing according to a state of significance flags of a bit to be processed and ambient bit group and a context and a decision of sign bits changing

according to a state of the sign bits of the bit to be processed and the ambient bit group; adopting the context and decision of the sign bits only when a value of the bit to be processed is 1 and updating the significance flag; disposing off the context and the decision when the value of the bit to be processed is 0; and updating a processed flag whether the value of the bit to be processed is 1 or 0;

a step of processing a magnitude refinement pass, wherein a second processing circuit of the bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said second processing circuit referring to significance second bit which is information about as to whether or not a bit to be processed is processed with the magnitude refinement pass at first time, a processed flag and an significance flag so as to make a judgment as to whether or not the bit to be processed is processed; and when the bit to be processed is processed with the magnitude refinement pass, generating a context and a decision of the bit so as to update the processed flag; and

a step of processing a cleanup pass, wherein a third processing circuit of the bit modeling, when all bits in Annie group to be processed are unprocessed, makes a judgment as to whether or not the bits can be processed collectively and when all the bits in the group are insignificant,

generating a special context and a decision, and does not process processed bits and processes insignificant bits, and wherein one bit when processing all the bits collectively and four bits when processing the bits in the same group are processed simultaneously and in parallel,

wherein, when the bit plane is same, then the significance propagation decoding pass, the magnitude refinement pass, and the cleanup pass are processed successively.

7. A processing method of JPEG 2000 bit modeling comprising:

a step of processing a significance propagation decoding pass, wherein a first processing circuit of bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said first processing circuit simultaneously generating a context and a decision of data changing according to a state of significance flags of a bit to be processed and ambient bit group and a context and a decision of sign bits changing according to a state of the sign bits of the bit to be processed and the ambient bit group; adopting the context and decision of the sign bits only when a value of the bit to be processed is 1 and updating the significance flag; disposing off the context and the decision when the value of the bit to be

processed is 0; and updating a processed flag whether the value of the bit to be processed is 1 or 0;

a step of processing a magnitude refinement pass, wherein a second processing circuit of the bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel, said second processing circuit referring to significance second bit which is information about as to whether or not a bit to be processed is processed with the magnitude refinement pass at first time, a processed flag and an significance flag so as to make a judgment as to whether or not the bit to be processed is processed; and when the bit to be processed is processed with the magnitude refinement pass, generating a context and a decision of the bit so as to update the processed flag; and

a step of processing a cleanup pass, wherein a third processing circuit of the bit modeling, when all bits in Annie group to be processed are unprocessed, makes a judgment as to whether or not the bits can be processed collectively and when all the bits in the group are insignificant, generating a special context and a decision, and does not process processed bits and processes insignificant bits, and wherein one bit when processing all the bits collectively and four bits when processing the bits in the same group are processed simultaneously and in parallel,

wherein, when the bit plane is same, three adjacent groups in said bit plane are processed in parallel for each of the significance propagation decoding pass, the magnitude refinement pass, and the cleanup pass.

8. The processing method according to claim 7, processing a plurality of bits in the bit plane in parallel.

9. The processing method according to claim 7, processing a plurality of bit planes in parallel.

10. The processing method according to claim 7, said processing circuit further comprising a register which stores data bits, sign bits, processed flags, significance flags and significance second bits for a code block size.

11. The processing method according to claim 7, each of said first, second, and third processing circuit further comprising a register which stores a data bit, a sign bit, a processed flag, a significance flag and a significance second bit for a bit to be processed.